

APPLICATION NOTE 1

SAVE HOURS OF VALUABLE TIME

This applications information is intended to save you hours (maybe days) of hard work and avoid many frustrating experiences with power circuits. We highly recommend that you take the small amount of time required to read this section so that you can avoid the common pitfalls in designing and testing power operational amplifier circuits. As a minimum, you should read all oblique print and the first paragraph in each numbered subsection. The majority of these problem areas have been identified from APEX Applications Hotline discussions of actual circuits. They range from higher than expected errors to total destruction of the amplifier.

1.0 ENVIRONMENTAL AND HANDLING PRECAUTIONS

Most of this document concerns design and application practices that will ensure the long and productive life of an Apex amplifier. However, not all design flaws can be seen on a schematic diagram. This is a list of the most serious handling and environmental hazards to an Apex product.

- 1) ESD - All Apex amplifiers should be handled using proper ESD Precautions. Many of our amplifiers include MOSFET devices which are particularly susceptible to damage from ESD.
- 2) Condensation - If the operating environment is capable of producing condensation on the amplifier use conformal coating to prevent a short between leads. The pin construction on the PowerSIP package is such that condensation can be trapped between the leads affecting performance and reducing the life of the device.
- 3) Compressible Thermal Washers - On package types with more than one point of attachment to a heatsink, compressible thermal pads can cause internal mechanical damage to the amplifier. There is more discussion in section 8.0.
- 4) Over-torque on the case - Follow the recommended torque guidelines when mounting screws are used to attach the package to the heatsink. There is more discussion in section 8.0.
- 5) Heatsink pin clearance - Be sure to protect pins from the heatsink. Use plastic or Teflon tubing on the pins to insulate them from the heatsink with packages requiring the pins to pass through the heatsink. There is more discussion in section 8.0.

2.0 BEFORE YOU APPLY POWER

In the design/prototype phase of an application, many dangers exist which will be eliminated by the time the circuit is ready for production. Pins may be wired in reverse order, connections may be missing, or test probes may cause momentary shorts. Any of these can destroy power amplifiers or other components in short order.

Five procedures can be employed to substantially reduce these dangers:

- 1) *Set power supplies to the minimum operating levels allowed by the data sheet.*
- 2) *Set amplifier current limit to very low levels (i.e. use a current limit resistor of approximately 2.2 ohms for high current models*

and 47 ohms for high voltage models). Consult Section 5, "Current Limit," as well as the individual data sheet to determine the proper values for the current limit resistor(s). Do not depend on the variable current limit feature of your lab power supply for protecting the amplifier.

It is much safer to install current limit resistors. Setting the current limit to a low value on a commercial lab supply will not protect the amplifier against the surge current available from the output filter capacitors. Even when average power dissipation is low, SOA violations can occur due to secondary breakdown of bipolar output stages. This mode of output stage destruction results from simultaneous application of high current and voltage to the conducting transistor. See Section 6 on SOA and the individual data sheets to better understand SOA limits.

- 3) *Check for oscillations.* With low voltage applied and reduced current limits in place, set the input signal to zero and connect a wide bandwidth (100 MHz or greater) oscilloscope to the output of the op amp. With the time base set to the microsecond region, check for oscillations present at any amplitude settings. Next, inject a signal into the circuit and monitor the output for oscillations. Excessive ringing on small signal square wave response indicates marginal stability.

If an oscillation is found, measure the frequency and amplitude of oscillation. Also note whether the oscillation only shows up on the positive or negative half of the output. Refer to Section 10, "Stability," for diagnosing and fixing the cause of instability.

With low voltage applied and reduced current limits in place, the basic function of the circuit can be verified. Once the circuit is operating as desired, raise the current limit and check worst case operating conditions, i.e. motor reversal, square wave drive of reactive loads, or driving the output to $V_s/2$ for resistive loads. Only then should you gradually raise the supply voltages to the maximum while checking worst case operation. This procedure not only saves many failures but it also helps to pinpoint problems to specific voltages and power levels.

- 4) *Use the largest possible heatsink for your prototype work.* This precaution provides the best environment to make thermal measurements on the case of the amplifier during worst case loading conditions without premature failures from thermal overload. Once you verify your calculations, you may decide to use a smaller heatsink for your final circuit. Consult Section 7, "**Internal Power Dissipation And Heatsinking**," for information on calculating heatsink requirements for your application.
- 5) *Avoid switching while the circuit is under power.* This includes plugging/unplugging banana jacks, switching relays in high current lines, switching within a feedback loop, etc. See Sections 9.1 and 9.3 for a further discussion of the dangers of switching.
- 6) When using an externally compensated amplifier, be aware that the compensation capacitor will be stressed to nearly the total supply voltage. A check of the equivalent circuit diagram will show one compensation terminal is within a few volts of one of the supply rails (often connected to the

gate of a FET) and the other is very close to the output voltage. At 300V and below, normal voltage margins are adequate. Above this it is advisable to rate the capacitor at twice the supply voltage. In this area, partial discharge and corona effect can take place. A good way to visualize the problem is to think of little packets of energy jumping across the capacitor. The FET gate can be destroyed long before incremental damage to the capacitor is ever seen.

3.0 ABSOLUTE MAXIMUM SPECIFICATIONS

Amplifiers should always operate below their Absolute Maximum Ratings to prevent permanent damage. If operation results in one of these maximums being reached, no permanent damage will result. *Simultaneous application of two or more of these maximum stress levels may result in permanent damage to the amplifier.* Note that proper operation is only guaranteed over the ranges listed in the Specifications table.

Example: Most amplifiers have an Absolute Maximum case temperature rating of +125°C. If the Specifications table gives an operating temperature range of up to +85°C, then the parameter limits in the Specifications table are not valid between +85°C and +125°C. In addition, the amplifier may not even be operational in this range, (for example, the amplifier may latch to one of its supply rails when above +85°C). However, the device will not sustain permanent damage unless the latched condition also violates the safe operating area.

The absolute maximum power dissipation rating used by APEX is the generally accepted industry method which assumes the case temperature of the amplifier is held at 25°C and the junctions are operating at the absolute maximum rating. This standardization provides a yardstick when comparing ratings of various manufacturers. However, it is not a reasonable operating point because it requires an ideal (infinite) heatsink. Furthermore, even with the best heatsink, *sustained operation at the maximum rated junction temperature will result in reduced product life.* Refer to Section 7, “**Linear Power Dissipation And Heatsinking**,” for information regarding operating junction temperatures and relative product life. APEX generally recommends operating at a case temperature that keeps maximum junction temperatures at 150°C or below.

Absolute Maximum Common Mode Voltage is another rating that illustrates the difference between the rated absolute maximum and the specified operating range. On many amplifiers, the rated absolute maximum voltage applied to both inputs simultaneously is equal to the power supply voltage. However, the linear operating range is 5V to 30V less than each power supply rail. This means that inputs exceeding the linear range specification will not damage the part but the amplifier may not achieve the specified rejection ratio, may start to distort the signal, or could even latch the output to one of the supply rails.

For more information on specifications and limits, see Section 9, “**Amplifier Protection And Performance Limitations**,” Section 6, “**SOA**,” Section 4, “**Power Supplies**,” and the “**Parameter Definitions**” section.

4.0 POWER SUPPLIES

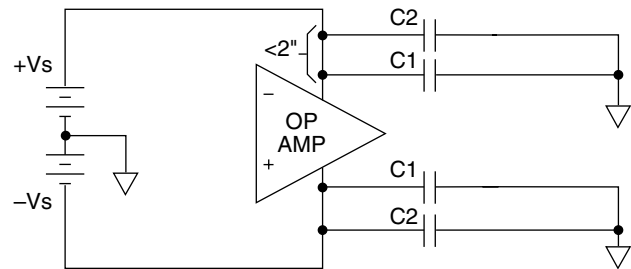
4.1 VOLTAGE SPECIFICATION

The specified voltage ($\pm V_s$) applies for a dual supply having equal voltages ($\pm 30V$). An asymmetrical (+50V/-10V) or a single supply (60V) may be used as long as the total voltage between +Vs and -Vs does not exceed the maximum rating. Never allow reverse voltage on a supply pin. On a dual supply circuit, do not operate with only one supply connected.

4.2 POWER SUPPLY BYPASSING

Inadequate power supply bypassing can lead to power amplifier circuit oscillations. Each supply pin should be bypassed to common with a “low frequency bypass” capacitance of 10 μ F per Ampere of peak output current. Tantalum capacitors should be used, although computer grade aluminum electrolytics can be substituted for operating temperatures above 0°C.

In addition, a “high frequency bypass,” .1 μ F to 1 μ F ceramic capacitor, should be added in parallel with the low frequency bypass capacitors from each supply rail to common. Refer to Figure 1. The ceramic capacitors must be mounted as close as possible (1/4" is good) to the supply pins. The larger capacitors should be within a few inches.



C1 = .1 to 1 μ F, Ceramic, High Frequency Bypass
C2 = 10 μ F/Amp out (peak), Electrolytic/Tantalum, Low Frequency Bypass

FIGURE 1. POWER SUPPLY BYPASSING

4.3 OVERVOLTAGE PROTECTION

The amplifier should not be stressed beyond its Absolute Maximum supply voltage rating. The amplifier should be protected against any condition that may lead to this voltage stress level. Two common sources of overvoltage are the high energy pulses from an inductive load coupled back through flyback diodes into a high impedance supply and AC main transients passing through a power supply to appear at the op amp supply pins.

Unipolar devices also protect against reverse polarity. Note that an open supply pin can cause supply reversal and sometimes amplifier destruction. *Transient suppressors with a voltage rating greater than the maximum power supply voltage expected but less than the breakdown voltage of the amplifier will prevent the amplifier from damage.*

Transients from the AC mains can be clamped through the use of MOVs (Metal Oxide Varistors) such as those made by General Electric, or bipolar TransZorbs. Connect either of these devices across the inputs to the power supply to reduce transients before they reach the power supply. Low pass filtering can be done between the AC main and the power supply to cut down on as much of the high frequency energy as possible. Note that inductors used in power supply filters will pass all high frequency energy and capacitors used in the filter are usually electrolytics which have high ESR. Because of this high ESR, high frequency energy will not be attenuated fully and therefore will avoid the capacitor with little reduction. Refer to Figure 2 (next page).

5.0 CURRENT LIMIT

The primary function of current limit is to keep an amplifier within its SOA. See Section 6, “**Safe Operating Area**.” Some models of Apex Power Op Amps have an internal current limit, while most of our models have an adjustable limit that is set with one or two external resistors.

Any attempt to limit current with a circuit external to the amplifier must be approached with extreme caution. The pitfalls are

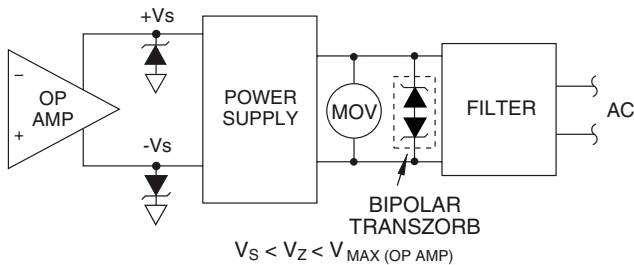


FIGURE 2. OVERVOLTAGE PROTECTION

generally time related and are often catastrophic. Most power supply current limit circuits are effective only AFTER stored energy in a large output filter capacitor has been depleted. This energy plus energy in local supply bypass capacitors is often more than enough to destroy the amplifier.

Slow response time is also a problem with even the fastest fuses. A 15 second response time to a 200% over current is common. In most applications the amplifier will give its life protecting the fuse. Even if the fuse does blow, the amplifier may still be damaged. The blowing fuse is a mechanical interruption in a current carrying line which can cause voltage spikes above the supply rating of the amplifier.

5.1 CURRENT LIMIT PRECISION

Standard current limit circuitry is not designed to provide a precision current limit function. A rule of thumb is to allow $\pm 20\%$ variation at room temperature. Furthermore, the current limit varies over temperature. This temperature dependence is generally shown in a typical performance graph in the product data sheet. Specific values of the nominal current at any given temperature may be calculated by modifying the 0.65V term of the current limit equation given in Section 5.3 with -2.2mV per degree (Centigrade) of case temperature rise above 25°C . For example, at a case temperature of 125°C , this term becomes 0.43V rather than 0.65V; $(650\text{mV} - (125^\circ\text{C} - 25^\circ\text{C})(-2.2\text{mV}))$. When working with high currents, the impedance of PCB traces, lead lengths and solder joints must be included in the current limit calculations.

5.2 EXTERNALLY ADJUSTABLE CURRENT LIMIT

Models with provisions to adjust current limit externally must have the current limit resistors connected as shown in the external connection diagram.

Current limit should never be set at a value greater than the rated maximum output current of the power op amp. This maximum is due to the current density limitations of conductors in the package and exceeding it can destroy the amplifier. Also, using a very low resistance (such as a jumper wire) will lead to increased bias current in the output stage. This raises power and temperature, while lowering resistance to second breakdown, thereby destroying reliability.

Operation without current limit resistors installed (current limit pins left open) can also cause failures, especially with inductive loads. This includes even a momentary open circuit while switching current limits with mechanical contacts. For the high current series power op amps, minimum programmed limits should be 20mA, while 10mA is minimum for most of the high voltage, low current series. Open circuits or limits below these minimums can cause voltage breakdown of the current limit transistors.

5.3 CALCULATING CURRENT LIMIT

Power op amps with provisions to adjust current limit externally require one or two current limit resistors (R_{CL}) which must

be connected as shown in the applicable external connection diagram below. Since output current flows through these resistors, wattage ratings must be considered. For optimum reliability, the resistor values should be set as high as possible. Some amplifier data sheets provide model specific equations, but in general each resistor and its power dissipation is calculated as follows:

$$R_{CL} \text{ (ohms)} = \frac{0.65}{I_{LIM} \text{ (A)}}$$

$$P_{R_{CL}} \text{ (watts)} = 0.65 \cdot I_{LIM}$$

I_{LIM} is the value of current limit desired and should be chosen to provide the amount of protection required for the specific application. For details on choosing "safe" levels of current limit and the protection/performance trade offs involved, see Section 6.3, "Fault Protection Using Current Limit."

For two resistor current limit schemes, asymmetrical current limiting ($R_{CL+} \neq R_{CL-}$) is permissible.

Foldover current limit, discussed in detail in AN #9, Current Limiting, provides a lower current limit for short circuit conditions while increasing current limit for load drive. APEX power amplifiers, the PA10, PA12 PA04 and PA05, have this feature. Foldover reduces the protection/performance trade-off inherent in setting current limit. The Power Design Tool will calculate and plot current limit on an SOA graph for most linear amplifier models. It is available free at www.apexmicrotech.com.

6.0 SAFE OPERATING AREA (SOA)

6.1 READING THE SOA GRAPH

The horizontal axis on the SOA curve, $V_S - V_O$, defines the voltage stress across the output device that is conducting. It does not define a supply voltage or total supply voltage or the output voltage. $V_S - V_O$ is the magnitude of the differential voltage from the supply to the output across the transistor that is conducting current to the load. Put another way: if the amplifier is sourcing current, use $(+V_S) - V_O$. If the amplifier is sinking current, use $(-V_S) - V_O$. Refer to Figures 3a & 3b.

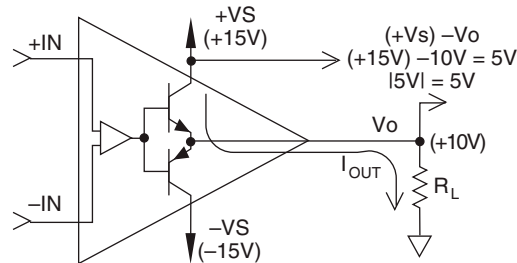


FIGURE 3A. SOURCING CURRENT

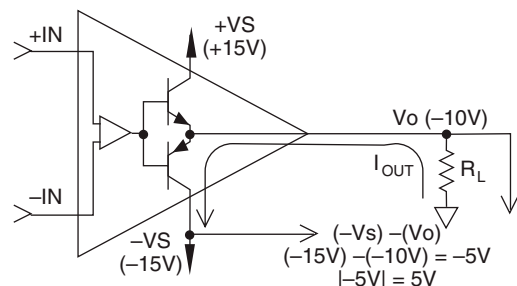


FIGURE 3B. SINKING CURRENT

The vertical axis represents the current that the amplifier is sourcing or sinking through the Output pin.

The Safe Operating Area curves show the limitations on the

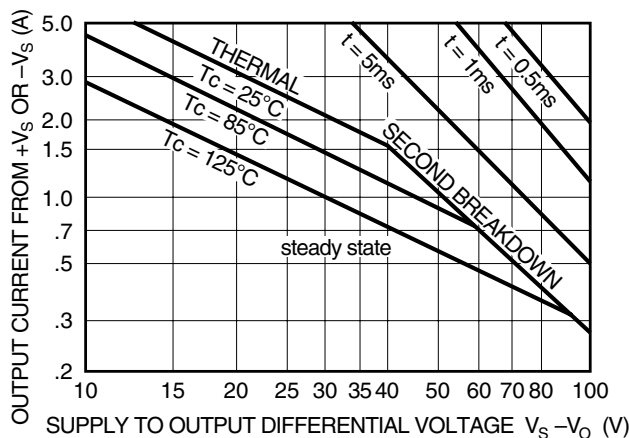


FIGURE 4. TYPICAL SOA CURVE

power handling capability of the amplifier. Refer to Figure 4. There are three basic limitations:

- 1) **Current handling capability.** This horizontal line near the top of the SOA CURVE represents the limit on output current imposed by current density constraints in the wire bonds, die junction area and thick film conductors.
- 2) **Power dissipation capability.** This is the power dissipation capability of the amplifier output stage. Note that the product of output current on the vertical axis and $V_S - V_O$ on the horizontal axis is constant over this line. In other words, this portion of the SOA curve is a “constant power line.” For $T_C = 25^\circ\text{C}$, this line represents the maximum power dissipation capability of the amplifier at maximum junction temperature using an infinite heatsink. As case temperature increases, this constant power/thermal line moves toward the origin. The new constant power line can be determined from the Power Derating curves on the data sheet. The case temperature is primarily a function of the heatsink used. For more details, refer to Section 7, “**Linear Power Dissipation And Heatsinking.**”
- 3) **Second Breakdown.** Second breakdown is a phenomenon exhibited by bipolar transistors when they are simultaneously stressed with high collector-emitter voltage and high collector current. Non-uniform current density in the emitter results in localized heating and “hot spots” at the junction. The temperature dependence of junction current results in increased current density at the hot spots. This concentration of current tends to further increase the temperature. The process is cumulative, leading to thermal runaway and transistor failure. Note that MOSFET power transistors do not have this second breakdown limitation.

The transient second breakdown lines ($t = 0.5\text{ms}$, $t = 1\text{ms}$, and $t = 5\text{ms}$) are based on a 10% duty cycle. For instance, in Figure 4, the amplifier may deliver 1.5A at a $V_S - V_O$ of 60V for 5ms but then must wait for 50ms before repeating this stress level. It is highly recommended to avoid entering the region beyond the DC second breakdown limits. Operation outside steady state limits in transient SOA regions is difficult to analyze adequately enough to insure best possible reliability.

6.2 HIGH SOA STRESS CONDITIONS

For resistive loads tied to ground, calculating power dissipation in the amplifier is reasonably simple. Refer to Section 7.1, “**DC Power Dissipation,**” and Section 7.2, “**AC Power Dissipation.**” However, with reactive loads, the voltage/current phase difference results in higher power being dissipated in the amplifier.

An example of an excessive transient stress condition cre-

ated by a capacitive load is shown in Figure 5a. In this case the capacitive load has been charged to $-V_S$. Now the amplifier is given a “go positive” signal. Immediately the amplifier will deliver its maximum allowed output current (I_{LIM}) into the capacitor, which can be modeled at time $t=0+$ as a voltage source. This leads to a voltage stress across the conducting device equal to the rail-to-rail supply voltage. Simultaneously, the amplifier will be conducting its maximum (current-limited) value of current.

Figure 5b shows a similar transient stress condition for an inductive load. For this situation we imagine the output is near the positive supply and current through the inductor has built up to some value I_{LOAD} . Now the amplifier is given a “go negative” signal which causes the output voltage to swing down to the negative supply. However, the inductor at time $t=0+$ can be modeled as a current source that requires the amplifier to continue to source I_{LOAD} . This leads to the same situation as before, that is, total supply voltage across a device conducting maximum rated current.

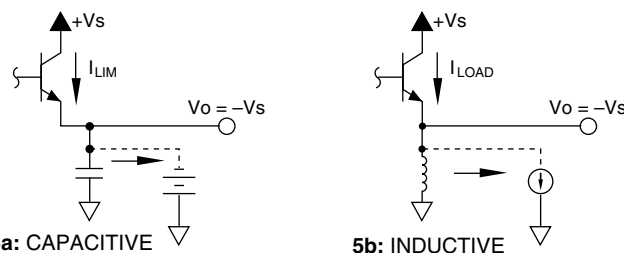


FIGURE 5. TRANSIENT STRESS WITH REACTIVE LOADS

Note also that reactive loads cause higher thermal stress levels than resistive loads even under steady state sinusoidal conditions. For purely reactive loads, all of the power is dissipated in the amplifier, none in the load.

6.3 FAULT PROTECTION USING CURRENT LIMIT

With a given supply voltage, current limit can be used to keep the amplifier within its Safe Operating Area. This allows amplifier protection during fault conditions such as shorts to ground or shorts to either supply. The cost of protection is lowered output current capability.

For short-to-ground fault protection, set current limit to the value given by the intersection of the supply voltage and the DC SOA curve for the appropriate case temperature. Simply find the supply voltage on the horizontal axis. When the output is shorted to ground, $V_O = 0$; therefore, $V_S - V_O = V_S$, follow up to the SOA curve intersection and then across to the output current. Referring to Figure 6, we see that in this example, a 2A current limit provides short circuit protection to ground at a case temperature of 25°C with $\pm 30\text{V}$ supplies. Note that better heatsinking allows higher values of current limit.

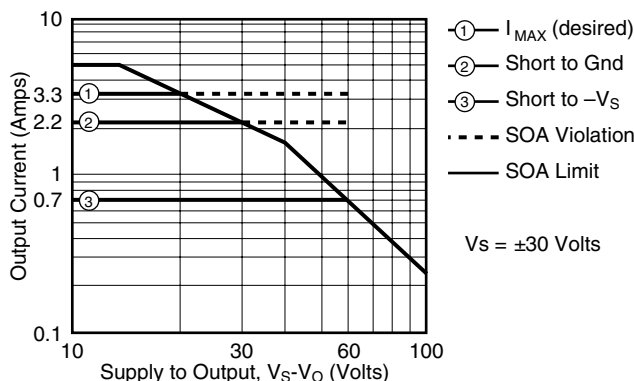


FIGURE 6. CURRENT LIMIT FAULT PROTECTION

For short-to-either supply protection, set current limit to the value given by the intersection of the rail-to-rail supply voltage (V_{SS}) and the DC SOA curve. This requires a significant lowering of current limit. For this type of protection, add the magnitudes of the two supplies used, find that value on the $V_S - V_O$ axis, follow up to the SOA limit for the case temperature anticipated, then follow across to find the correct value of current limit. Referring to Figure 6, we see that in this example, a 0.7A current limit allows short protection to either supply.

It is often the case that requirements for fault protection and maximum output current may conflict. Under these conditions there are only four options. The first is to simply go to an amplifier with a higher power rating. The second is to trim some of the requirements for fault protection. The third is to reduce the requirement for maximum output current. The fourth option is a special type of current limit called “foldover” or “foldback.” This is available on some amplifiers such as the PA10 and PA12. For a detailed discussion of foldover current limit and SOA fault protection refer to Application Note 9, “**Current Limiting.**” For an explanation of how to choose current limit resistors to adjust current limit, see Section 5.3, “**Calculating Current Limit.**”

7.0 LINEAR POWER DISSIPATION AND HEATSINKING

It is important to not confuse Internal Power Dissipation with power delivered to the load. These two power levels are equal only at unique signal levels. Low impedance faults or highly reactive loads will likely result in internal power dissipation being the higher level. Well-designed circuits with less reactance will yield higher efficiency.

There are two main steps in the heatsink selection process. First, the maximum internal power dissipation must be calculated. Secondly, the maximum desired junction and case temperatures must be chosen and the thermal model used to calculate the required thermal conductance of the heatsink. The following four sub-paragraphs deal with finding internal power dissipation in the output transistors generated by delivering current to the load only.

For purposes of power dissipation calculation, DC refers to any signal with a frequency below 60HZ. At true DC, heat is generated in only one output transistor and ability to conduct this heat to the surface of the amplifier case is determined by thermal conductance of materials and square area. As frequency increases, our original transistor now has a time variable heat load and the opposite side output transistor now generates the heat on alternate half cycles. This means the wattage figure can move from peak value toward RMS and more square area is used to conduct heat to the case, implying a lower thermal resistance. At 1HZ, internal thermal time constants are so fast compared to the half-second duration of the conduction cycle of each transistor, that no advantage gained. At 1KHZ, conduction cycles are short compared to internal time constants and thermal averaging allows taking advantage of both RMS power levels and the lower thermal resistance. While physics produces a smooth curve between these frequencies, the math is quite cumbersome. Most manufacturers of power op amps have adopted the 60HZ rule: Below 60HZ, use peak power and DC thermal resistance; otherwise use RMS power and AC thermal resistance.

7.1 DC POWER DISSIPATION

Power in the output transistor is the output current multiplied by the voltage across that transistor, or supply-to-output differential, $V_S - V_O$. For a purely resistive load, maximum power

dissipation occurs at $V_O = 1/2V_S$ and has a value of:

$$PD \text{ (max)} = \frac{V_S^2}{4R_L} \text{ [Purely resistive load only]}$$

Where:

V_S is the supply magnitude of the conducting transistor.

R_L is the load resistance.

For AC signals below 60HZ driving reactive loads, plot the load line to find stress levels. Use the highest power level from the plot for heatsink selection. Application Note 22 discusses SOA and Load Lines. As an example, consider the PA12A, $\pm 48V$ supplies, $\pm 40V$ signal at 50HZ driving a 69mH coil with 12.5 Ω resistance, mounted on a 0.3 $^{\circ}C/W$ heatsink. Figure 7 is the load line for this circuit with peak internal dissipation of 67.5W at 1.28A. Load impedance is 25 Ω at 60 $^{\circ}$ resulting in apparent power of 32VA and a power factor of 0.5. Quite a limitation for an amplifier boasting an ABSOLUTE MAXIMUM RATING of 125W! The software secret behind this plot will be revealed later.

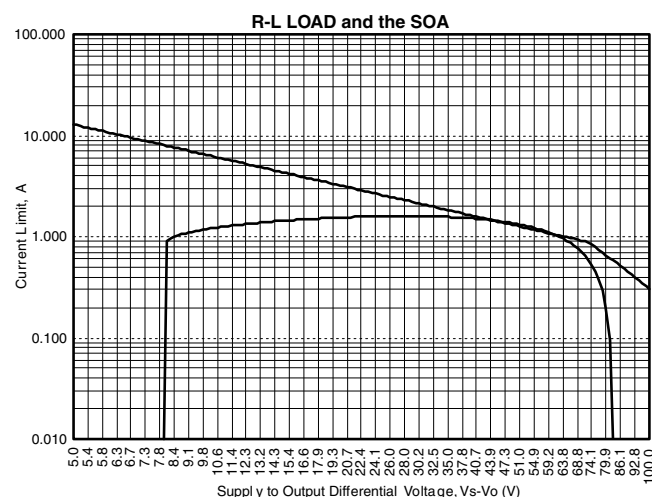


FIGURE 7

ELECTRICAL MEASUREMENT METHOD

Although we present this under the DC heading and it is primarily used at low frequencies, instrumentation errors are the only limitations on frequency. The ideal way to run this test is to have an amplifier/heatsink combination you are certain is large enough to handle all the power. While this may sound like circular cells in a spreadsheet, the test still has its place. Many loads do not change impedance with changing drive amplitude. If this is true, it is possible to replace the power amp in Figure 8 (next page) with a signal generator or a low power amplifier. Set the drive signal to a convenient fraction of the ultimate level, and rescale the voltages and currents measured prior to calculating power levels. If using a programmable signal generator, the actual output amplitude is not likely to match the programmed level because the load impedance is not likely to match the generator output impedance.

1. Use a small value current sense resistor between the load and ground to develop a voltage proportional to I_L . Use this signal to drive one channel of the X-Y display of an oscilloscope.
2. Use the output voltage of the amplifier, V_O , to drive the other channel of the X-Y display.
3. Calculate instantaneous power dissipation in the amplifier for several points on the ellipse using:

$$PD_{OUT} = (V_S - V_O) I_{LOAD}$$

4. Plot the points on the SOA curve and check for violations.

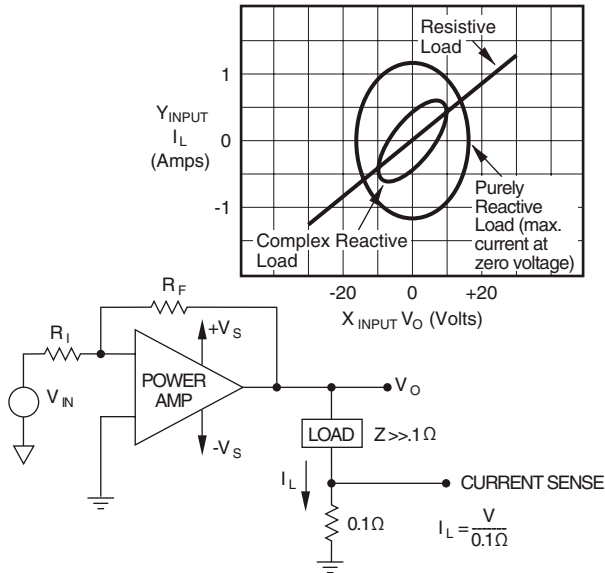


FIGURE 8. AC PD_{OUT}: ELECTRICAL MEASUREMENT

7.2 AC POWER DISSIPATION

Again, “AC” for the purpose of determining power dissipation means at least 60HZ. For the moment, we will also confine the discussion to sinusoidal signals and symmetric supplies. Starting with the simple: When driving a pure resistance, power dissipation is maximum when the sine wave peak is $0.637 \cdot V_s$. Refer to Figure 9 to see how the heat load on the amplifier decreases as signal amplitude varies in either direction. This equation yields maximum power:

$$PD(\max) = \frac{2V_s^2}{\pi^2 R_L} \text{ [Purely resistive load only]}$$

Where:

- V_s is the magnitude of each supply.
- R_L is load resistance.

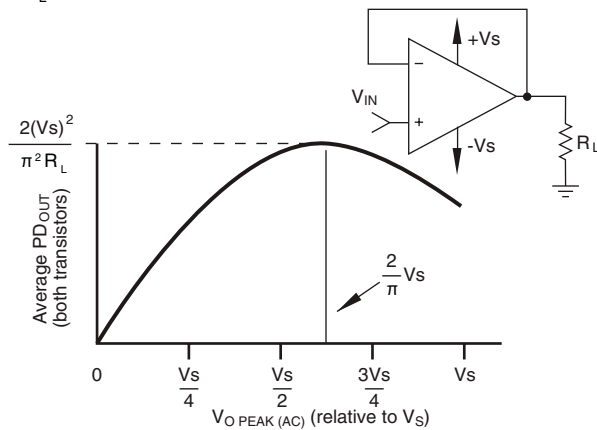


FIGURE 9. AC POWER DISSIPATION VS. PEAK OUTPUT VOLTAGE

SIMPLE APPROXIMATION FOR REACTIVE LOADS

As loads move from pure resistance toward pure reactance, three changes should be noted:

- 1) The fraction of V_s corresponding to maximum power dissipation goes from 0.637 toward one. See Figure 10.
- 2) Power factor goes from one toward zero. With a pure reactance, no heat is generated in the load (no work is done).

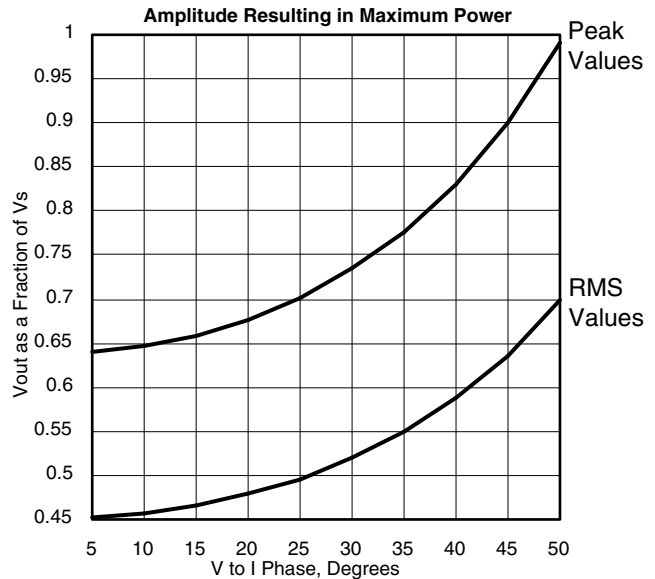


FIGURE 10. AMPLITUDE PRODUCING MAXIMUM POWER MOVES WITH PHASE ANGLE

- 3) The difference between load VA and true watts is dissipated in the amplifier.

Even with these changes, one of the two following formulas can be used to approximate internal power dissipation. The key is knowing the phase difference between V & I in the load, to find the power factor, $\text{COS}\phi$, where ϕ is the angle between the voltage and the current. With only one reactive element in the load it is easy to determine what frequency will produce the largest power dissipation. With the power factor and load impedance measured or calculated, the formulas are:

$$PD(\max) = \frac{2V_s^2}{\pi^2 Z_L \text{COS}\phi} \text{ [Primarily resistive loads, } \phi < 40^\circ \text{]}$$

$$PD(\max) = \frac{V_s^2}{2 Z_L} \left[\frac{4}{\pi} - \text{COS}\phi \right] \text{ [Primarily reactive loads, } \phi > 40^\circ \text{]}$$

Where:

- V_s is the magnitude of each supply.
- Z_L is load impedance magnitude.

MORE ACCURATE METHODS

This method can be used analytically or on the bench as long as the test amplifier and heatsink are large enough to accommodate any errors in the first pass estimate of the circuit operation. Just as in the previous method, phase angle of the load must be known. Not only is it a term of the equations, but it is needed to determine the proper signal amplitude. Find the maximum power producing amplitude from Figure 10. If this is lower than the maximum amplitude your circuit will drive, use it. If not, use the circuit maximum.

- 1) Find the power delivered TO the amplifier from the supply:

$$P_{IN} = \frac{2V_S I_{S\text{PEAK}}}{\pi}$$

- 2) Find the power delivered from the amplifier to the load:

$$P_{OUT} = (1/2)V_{PEAK} I_{PEAK} \text{COS}\phi$$

- 3) Calculate power left in the amplifier:

$$PD_{INT} = P_{IN} - P_{OUT}$$

7.3 “OTHER” POWER DISSIPATION

For waveforms other than sinusoids, or for more complex energy storing loads such as motors, a Spice analysis and an

electrical test method as described under DC Power Dissipation is recommended. Application Note 24, Brush Type DC Motor Drive may also prove useful.

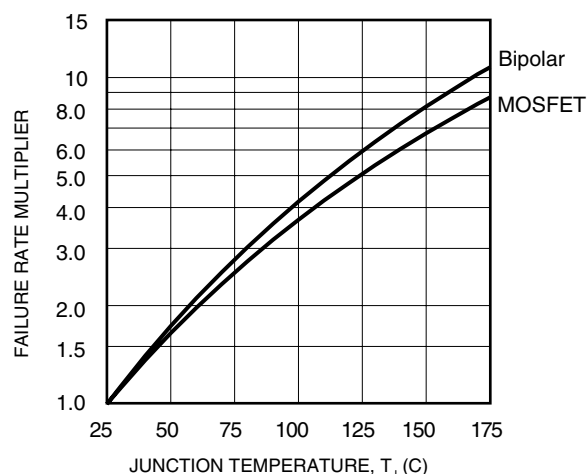
7.4 "EASY" POWER DISSIPATION

Power Design is an Excel spreadsheet available free from www.apexmicrotech.com. It remembers all the rules and formulas presented here, has a data base of model capabilities and finds the critical phase angle for you. Answers for simple loads are tabulated and load line plotted as fast as you can enter the data. Frequency sweeps on up to 54 component complex loads take a little longer. It also does calculations in the following paragraphs on heatsink selection plus, has sheets for stability, model selection, PWM filters and PWM power dissipation.

7.5 WHERE TO SET T_J MAX

For that matter, what is T_Jmax? In the ABSOLUTE MAXIMUM RATINGS area of a data sheet, it is the temperature limit set by the transistor manufacturer to insure leakage of that transistor does not become destructive. Especially on older bipolar models, 200°C appears frequently. This is not a good place to be on a continuous basis. From here on, T_J max will mean the design maximum for the circuit.

Reliability is a strong function of temperature. Figure 11, based on data from MIL-HDBK-217F, shows that a bipolar transistor operated a junction temperature of 175°C will have a mean failure rate more than ten times higher than with a junction temperature of 25°C. A MOSFET can be expected to fail almost nine times as often with the same temperature rise.



This data has been extracted from the base failure rate tables of MIL-HDBK-217F, revision of 2 December 1991.

FIGURE 11. MTTF VS. TEMPERATURE

Apex has seen applications required by military contract to meet a T_J max of 100°C. More often the designer must set T_J max based on application details. Would failure eliminate one bell or whistle on a non-critical piece of equipment, or completely stop a \$1M per hour production line? How about consequential damage? Is the amplifier used for 30 seconds each day, or continuously? Can the amplifier be easily replaced, or does this require a space vehicle? Simply trade off these concerns against time, size, weight and cost budgets to arrive at the perfect T_J max.

There are three approaches to lowering junction temperatures. The first is to lower internal power dissipation. Application Note 8, Optimizing Output Power, Notes 3 and 20 on bridge circuits and AN26 on parallel operation may prove helpful here. The second method is to lower the ambient temperature. This may involve placement choices inside an equipment enclosure

or the use of a chilled liquid cooling system rather than air-cooling. Last on the list, we must minimize thermal resistance from the transistor junctions to the ambient environment.

7.6 THERMO-ELECTRIC MODELS

Thermo-electric models translate power terms into their electrical equivalent. In these models, power is modeled as current, temperature as voltage and thermal resistance as electrical resistance. Since 1980, Apex has advocated using a simplified calculation of case and junction temperatures of power op amps. This shortcut assumed quiescent power was added to power dissipated due to output current and the total is used to calculate both temperatures. This yields the correct case temperature but predicts output transistor junction temperatures higher than the real world. This error is in the safe direction and generally insignificant until the amplifier combines high voltage and high speed causing quiescent power to be a significant percentage of the power rating of the output transistors alone.

The more accurate model shows that adding all the quiescent power to the calculation for the output transistors is an error because quiescent power is spread among all the components of the amplifier. From the data sheet point of view, the POWER DERATING graphs show power handling capability of the output transistors only, but the simple method produces a temperature rise in the output transistors due to current which does not flow in them. In the PA94, maximum quiescent current times maximum supply voltage develops 21.6W, over 70% of the power rating of the output stage. However, less than 1% of this power is in the output stage and the simple method imposes a false but severe limitation on power handling capability of the output transistors. It is very easy to design a reliable PA94 circuit where total power dissipation is greater than that allowed by the POWER DERATING graph.

THE SIMPLE MODEL

In Figure 12, P_D is the total power dissipation, that is P_D (internal dissipation of the output transistors due only to output current) plus quiescent power of the amplifier. Quiescent power (PD_Q) is quiescent current (I_Q) * total supply voltage.

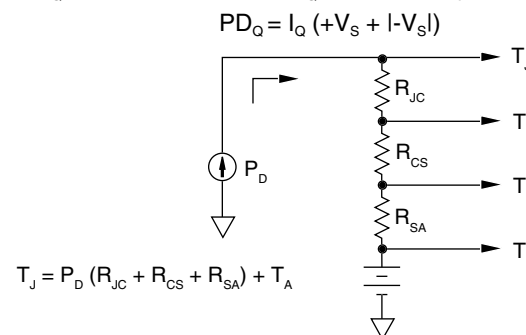


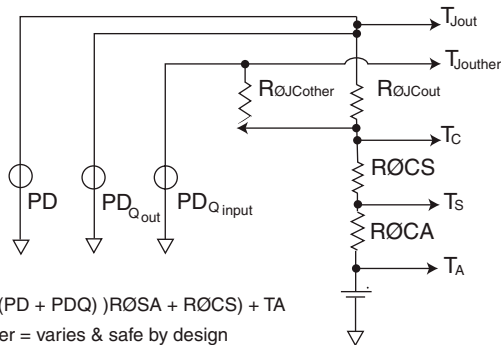
FIGURE 12. SIMPLE THERMO-ELECTRIC MODEL

A MORE ACCURATE MODEL

In Figure 13 (next page), quiescent power has been split according to the actual transistors generating the heat. PD_{Qout} is only the quiescent current flowing in the output transistors. When appropriate, this specification will appear in the amplifier data sheet. Multiply this output stage quiescent current times the total supply to find worst case PD_{Qout}.

$$PD_{Qout} = I_{Qout} (+V_S + |V_S|)$$

PD_{Qother} is the current flowing in all the other components and could be found by subtracting PD_{Qout} from PD_Q.



$$T_C = (PD + PD_Q) R_{\Theta SA} + R_{\Theta CS} + T_A$$

$$T_{Jother} = \text{varies \& safe by design}$$

$$T_{Jout} = (PD + PD_{Qout}) R_{\Theta JC} + (PD + PD_Q)(R_{\Theta SA} + R_{\Theta CS}) + T_A$$

FIGURE 13. MORE ACCURATE THERMO-ELECTRIC MODEL

Note that the data sheet junction-to-case thermal resistance speculations refer to only the output transistors. Thermal resistances and power dissipations of other components vary wildly. Design rules applied by Apex for all these components insure they will be reliable when operating within maximum supply voltage, maximum input voltage and maximum “Meets full range specifications” case temperature.

No matter which model you use, there are three thermal resistances contributing directly to hot junctions. The thermal resistance should be attacked on all three fronts:

- 1) Buy an amplifier with the lowest possible $R_{\Theta JC}$.
- 2) Use good mounting practices-see section 8 below.
- 3) Use the largest practical heatsink.

The amplifier is often a large portion of the thermal resistance budget. Better amplifiers usually cost more and sometimes are larger. Increased amplifier size is usually of little concern when compared to the size and weight of an adequate heatsink solution. If a larger amplifier can eliminate the need for liquid cooling or a fan, increased amplifier cost may not even be an issue. A reasonable starting point for amplifier selection is to find an ABSOLUTE MAXIMUM RATING of twice the power the circuit will actually dissipate.

$R_{\Theta CS}$ is often overlooked, but consider this: The PA12 with a AC thermal resistance of $0.9^{\circ}\text{C}/\text{W}$ is mounted on the HS11 liquid cooled heatsink boasting thermal resistance of $0.1^{\circ}\text{C}/\text{W}$. If T_A is 25° and $R_{\Theta CS}$ is 0.1, 125W will place junctions at 162.5°C . If a mica or plastic washer is used or the amplifier is mounted bare, power to maintain this junction temperature could be cut to less than 70W! Again, see section 8 below.

The heatsink performance is the last element of the thermal resistance challenge. A quick glance at an SOA curve showing the power handling difference between case temperatures of 85°C and 125°C tells a story; but not the whole story. Data sheet SOA curves always assume T_{Jmax} is allowed to go to the ABSOLUTE MAXIMUM RATING. If your design is more conservative, the difference in power ratings will be even larger. Also be aware that heatsink ratings should be viewed more a guideline than an absolute.

7.7 HEATSINK SELECTION

Let’s start with “the” heatsink rating. The HS03 is rated at $1.7^{\circ}\text{C}/\text{W}$ in free air. True, when power dissipation is about 45W, but check the actual curve at 10W and you’ll find a rating more like $2.3^{\circ}\text{C}/\text{W}$. On top of that, “free air” means no obstructions to air flow and the flat mounting surface must be in the vertical plane. Demands for higher performance in smaller packages can be at odds with optimum heatsinking. Poor installation choices can easily reduce effectiveness 50%.

Adding a fan to your design improves the thermal resistance

rating of heatsinks. Please remember: Most fans are rated in cubic delivery and this rating varies with working pressure. A 5-inch diameter fan delivering 100 CFM produces over 700 FPM right at the fan. If this air flows through a 19 x 24 inch rack, theoretical velocity is down to 32 FPM, will vary with location and goes lower as the rack is sealed tighter.

The bottom line: Without case temperature measurements, your design effort is NOT complete!

There are two temperature limitations on power amplifiers. A rating for each limitation must be calculated and numerically lower rating used. The most obvious limitation is the junction temperature of the output transistors. The case temperature must also be limited. In addition to reliability concerns (Figure 11 applies to the front end transistors as well as the output stage), DC error budget items of voltage offset drift and bias current drift are based on case temperature. Allowing a case temperature of 85°C as opposed to 40°C will increase voltage offset change by a factor of 4 and may double the failure rate of front end semiconductors. This would be a good time to recommend reading section 3 where the difference between ABSOLUTE MAXIMUM RATINGS and “Meets full range specifications” is discussed.

Here are some case-to-heatsink thermal resistance ratings ($R_{\Theta CS}$) of various package styles. These ratings assume the amplifier is mounted with either an Apex aluminum thermal washer or with a thin coating of fresh thermal grease covering the entire mounting surface. If designing the mounting surface, see the ACCESSORIES INFORMATION data sheet for recommended hole sizes.

TO-3	MO-127	PD10	SIP02,3	SIP12, 04, 5 (Kapton)
$0.1^{\circ}\text{C}/\text{W}$	$0.05^{\circ}\text{C}/\text{W}$	$0.08^{\circ}\text{C}/\text{W}$	$0.1^{\circ}\text{C}/\text{W}$	$0.2^{\circ}\text{C}/\text{W}$

Using either thermal model, the heatsink rating based on case temperature limitations is:

$$R_{\Theta SA} = \frac{T_C - T_A}{PD + PD_Q} - R_{\Theta CS}$$

Where:

T_C = maximum case temperature allowed.

PD = output transistor power dissipation due to load current

PD_Q = Total quiescent power.

THE SIMPLE METHOD

If PD_Q is one tenth of less PD , this simple method will work well. If the amplifier has a slew rate of several hundred volts/microsecond and the application is above 300V, use the more accurate method. The simple formula is:

$$R_{\Theta SA} = \frac{T_J - T_A}{PD + PD_Q} - R_{\Theta JC} - R_{\Theta CS}$$

Where:

T_J = maximum junction temperature allowed

$R_{\Theta JC}$ = AC or DC thermal rest from the specification table

THE MORE ACCURATE VERSION

With the unique combination of high voltage and speed such as the 900V and 500V/us of the PA94, traditional formulas for heatsink selection will falsely lower the apparent power handling capability of the amplifier. To more accurately predict operating temperatures use the following procedure.

Look for an output stage only quiescent current rating in the data sheet. If the data sheet does not list this specification, it can be estimated as 5% of the total quiescent current.

Find output stage quiescent power (PD_{QOUT}) by multiplying the output stage only quiescent current by the total supply (V_{SS}). Calculate a heatsink rating which will maintain output transistor junctions at 150°C or lower:

$$R_{\theta SA} = \frac{T_J - T_A - (PD + PD_{QOUT}) \cdot R_{\theta JC}}{PD + PD_Q} - R_{\theta CS}$$

Where:

T_J = maximum junction temperature allowed.

$R_{\theta JC}$ = AC or DC thermal resistance from the specification table.

THE EASY AND ACCURATE METHOD

- 1) Set aside the slide ruler and calculator.
- 2) Start Power Design, an Excel spreadsheet available free from www.apexmicrotech.com
- 3) Enter amplifier, V_{SS} , min/max frequency, output amplitude and load components.
- 4) Read load, supply and amplifier power levels, heatsink rating & maybe some warnings.
- 5) Tweak design as desired.
- 6) Enter design notes and press Print button for documentation.
- 7) Ask your boss for a raise.

8.0 AMPLIFIER MOUNTING AND MECHANICAL CONSIDERATIONS

For Power Op Amp designs, high reliability consists of mechanical considerations as well as electrical considerations. Proper mounting is very important for power amplifiers. Once the proper heatsink has been selected as described in Section 7, the following mounting techniques should be used.

All APEX metal can products have either an isolated case, ground connected case or a dedicated pin for the case. This means electrical insulating washers are generally not necessary and will likely increase operating temperatures if used.

In addition, APEX uses a thin beryllia substrate to get the lowest possible thermal resistance. While this leads to cool running, high reliability amplifiers, it is important not to run the risk of cracking this substrate. In order to prevent this, two major precautions must be observed:

- 1) *Do not use compressible thermal washers.* These are silicon rubber based pads such as Silpad. The amount of compressibility in a washer over 2 mil thick can lead to header flexing, which can crack the substrate. *The use of these washers voids the warranty.* Also, thermal grease has superior thermal properties.
- 2) When using reflow soldering with package types DF (PSOP1), DK (PSOP2), EF (QFP01) and EK (QFP02), be aware that these packages are moisture sensitive. These devices should be baked at 125°C for 48 hours and the reflow operation should be performed within 48 hours of baking. Black carriers (EF and EK packages) are suitable for baking. Clear plastic tubes (DF and DK packages) are NOT suitable for baking; the devices need to be removed from these tubes prior to baking. Caution must be exercised to avoid mechanical or ESD damage.
- 3) *Do not over torque the case.* Recommended mounting torque for the TO-3 and SIP packages is 4-7 in-lbs (.45-.79 N-m) and for the MO-127 Power Dip™ packages (PD10 AND PD12) is 8-10 in-lbs (.90-1.13 N-m). Refer to Figure 14. Apply a thin, uniform film of thermal grease or an Apex thermal washer between the case and heatsink. Apply small increments of torque alternately between each screw when mounting the amplifier.

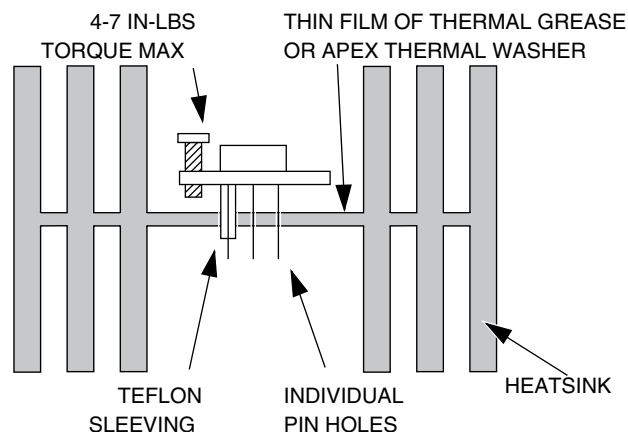


FIGURE 14. MOUNTING CONSIDERATIONS

Due to dimensional tolerances between heatsink thru-holes and power op amp packages, extreme care must be taken not to let the pins touch the heatsink inside the thru-holes. *Do not count on the anodization for insulation* as it can nick easily, exposing bare aluminum, an excellent electrical conductor. Use plastic tubing to sleeve at least two opposite pins if you are using a mating socket or printed circuit board. If you are wiring directly to the pins, it is best to sleeve all pins. Refer to the Package and Accessories Information section of the Hybrid & IC Handbook for further details on sleeving sizes, mating sockets and cage jacks for PC board mounting of power amplifiers. While teflon covers virtually all applications, the actual requirements are to withstand the maximum case temperatures and total supply voltage of the application.

Never drill out the entire area inside the pin circle, drill individual holes for each pin. Often, heatsinking is accomplished with a custom heatsink or by directly mounting to a bulkhead. These approaches require the use of heatsink thru-holes for the amplifiers pins. For the 8-Pin TO-3 package, the main path for heat flow occurs inside the circumference of 8 pins. Refer to Figure 15. Therefore, a single, large hole, to allow the 8 pins to pass through, will remove the critical heatsinking from where it is most needed. Instead, 8 separate #46 drill size holes must be drilled.

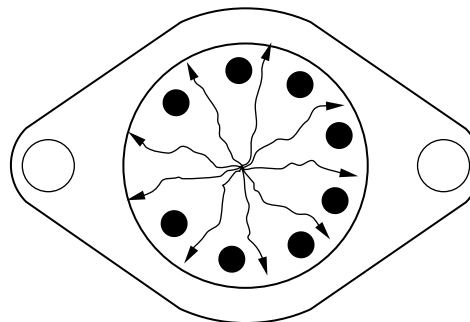


FIGURE 15. MAIN HEAT FLOW PATH: 8-PIN TO 3 PACKAGE

9.0 AMPLIFIER PROTECTION AND PERFORMANCE LIMITATIONS

9.1 OUTPUT PROTECTION

Attempting to make sudden changes in current flow in an inductive load will cause large voltage flyback spikes. These flyback spikes appearing on the output of the op amp can destroy the output stage of the amplifier. Brush type DC motors can produce continuous trains of high voltage, high frequency

kickback spikes. In addition, mechanical shocks to a piezoelectric transducer will cause it to generate a voltage. Again, this can destroy the output stage of an amplifier.

Although most power amplifiers have some kind of internal flyback protection diodes, these internal diodes should not be counted on to protect the amplifier against sustained high frequency, high energy kickback pulses. Many of these diodes are intrinsic "epi" diodes that occur as a result of the manufacture of the power darlington output transistor. Epi diodes generally have slow reverse recovery times and may have large forward voltage drops. Under sustained high energy flyback conditions, high speed, fast reverse recovery diodes should be used from the output of the op amps to the supplies to augment the internal diodes. See Figure 16. These fast recovery diodes should have reverse recovery times of less than 100 nanoseconds and for very high frequency energy should be under 20 nanoseconds.

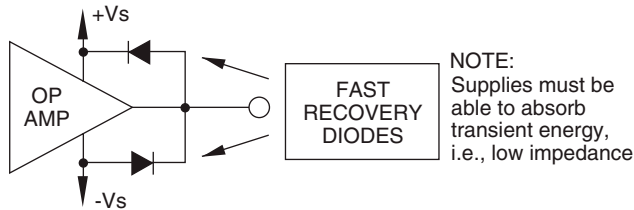


FIGURE 16. OUTPUT PROTECTION

One other point to note is that the power supply must look like a true low impedance source when current flows in the opposite direction from normal. Otherwise, the flyback energy, coupled back into the supply pin, will merely result in a voltage spike at the supply pin of the op amp. This would lead to an overvoltage condition and possible destruction. Refer to Section 4.3 for information on overvoltage protection.

9.2 COMMON MODE VOLTAGE LIMITATIONS

One of the most widely misunderstood parameters on an op amp data sheet is the *Common Mode Voltage Range*, which specifies how close an input voltage *common to both inputs* may approach either supply rail. When these limits are exceeded, the amplifier is not guaranteed to perform linearly. The *Absolute Maximum Common Mode Voltage* specification on most data sheets refers to the voltage above which the inputs may not exceed or damage will result to the amplifier.

There are two cases which clearly illustrate the constraints of common mode voltage specifications: single supply operation and asymmetrical supply operation.

Example:

The APEX PA82J has a Common Mode Voltage Range of $\pm V_S - 10$. This implies that if the PA82J is to be operated from a single supply, both inputs must be biased at least 10 volts above ground. Figure 17 illustrates an implementation of this which keeps both inputs above 10 volts for the given range

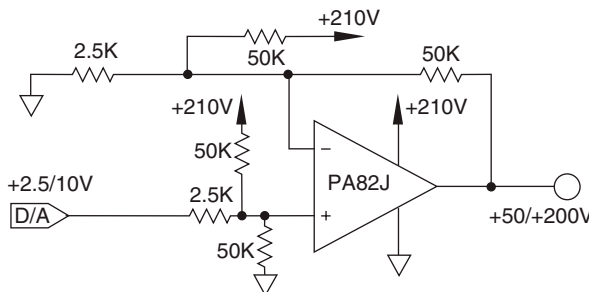


FIGURE 17. SINGLE SUPPLY OPERATION: V_{CM} CONSIDERATIONS

of input voltages. Note that for single supply operation, the output of the amplifier is never capable of swinging all the way down to ground. This is due to the output saturation voltage of the amplifier.

Figure 18 illustrates a very practical deviation from true single supply operation. The availability of the second low voltage source allows ground (common) referenced signals but also maximizes the high voltage capability of the unipolar supply. As long as the amplifier remains in the linear region of operation, the common mode voltage will be zero. With the 12V supply the allowed positive common mode voltage range is from 0 to 2V. Note the output of the PA81J can swing all the way to zero now also. The 12V supply in this case need only supply the quiescent current of the power op amp. If the load is reactive or EMF generating, the low voltage supply must also be able to absorb the reverse currents generated by the load.

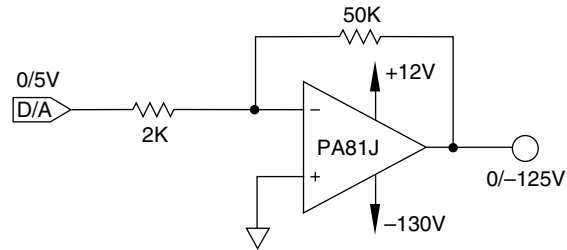


FIGURE 18. NON-SYMMETRICAL SUPPLY OPERATION

9.3 DIFFERENTIAL INPUT VOLTAGE LIMITATIONS AND PROTECTION

Exceeding the *Absolute Maximum Differential Input Voltage* specified on the data sheet can cause permanent damage to the differential input stage. Failure modes range from increased V_{OS} and V_{OS} drift, I_B and I_B drift, and input offset current, up to input stage destruction. Although the differential input voltage (V_{ID}) under normal closed loop conditions is microvolts, several conditions can cause it to be in the Volt range. Causes of V_{ID} :

- 1) Fast rise-time inputs.
- 2) Signal input while not under power.
- 3) High impedance output states (current limit, thermal shutdown, sleep mode).
- 4) Switching within the feedback loop.

An example of condition 4 is shown in Figure 19a.

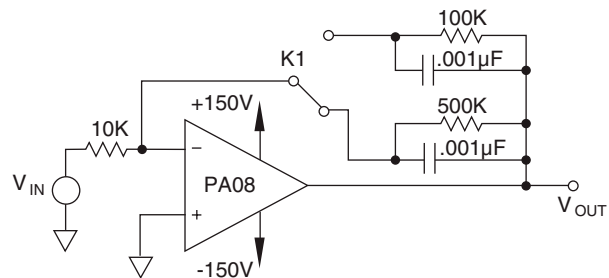


FIGURE 19a. GAIN SWITCHING AND V_{ID} VIOLATION

This configuration is often used in ATE systems for changing the gain of an op amp. The amplifier's full scale transition time (microseconds) is faster than the typical relay switching time (milliseconds); therefore when the relay opens the feedback loop, the AOL of the amplifier will drive the output to one of the supply rails. In the example shown, the output will approach 150V while the relay is still switching. Because the 100K feedback resistor has completely discharged its associated rolloff capacitor, the relay will connect 150V directly to the

input. Since the Absolute Maximum V_{ID} for the PA08 is $\pm 50V$, the input stage will be destroyed.

Effective input protection networks provide two functions:

- 1) Limit differential voltage to less than the reverse breakdown voltage of the input transistors base-emitter junction, typically $\sim 6V$.
- 2) Limit input transient current flow to less than 150mA.

Figure 19b shows an example of an input V_{ID} protection network. The diodes should be high speed devices such as 1N4148 and the series impedance should limit instantaneous current to a maximum of 150mA.

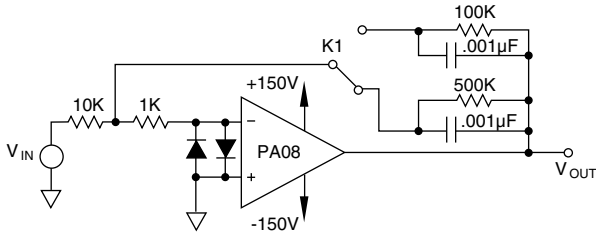


FIGURE 19b. GAIN SWITCHING AND V_{ID} PROTECTION

10.0 STABILITY

The most common application problem when working with power op amps is stability. Although most power op amps are compensated for unity gain stability, they are frequently required to drive reactive loads, deliver high currents, or use high impedances due to high voltage. These conditions make stability more difficult to achieve. However, EVERY circuit can be stabilized if the guidelines given here are followed. Table 1 provides a troubleshooting guide for stability problems. The “Probable Cause / Possible Solution Key” gives insight

CONDITION AND PROBABLE CAUSE TABLE			Oscillates unloaded? Oscillates with $V_{IN} = 0$? Loop Check† fixes oscillation? Probable Cause(s) (in order of probability)			
Oscillation Frequency	f_{osc}	UGBW	N	Y	N	
CLBW	f_{osc}	UGBW	N	Y	N	A, C, D, B
CLBW	f_{osc}	UGBW	Y	Y	Y	K, E, F, J
CLBW	f_{osc}	UGBW	—	N	Y	G
	f_{osc}	CLBW	N	Y	Y	D
	$f_{osc} =$	UGBW	Y	Y	N*	J, C
	$f_{osc} \ll$	UGBW	Y	Y	N	L, C
	$f_{osc} >$	UGBW	N	Y	N	B, A
	$f_{osc} >$	UGBW	N	N**	N	A, B, I, H

TABLE 1.

CLBW = Closed Loop Bandwidth

UGBW = Unity Gain Bandwidth

† See Figure 20 for loop check circuit.

— Indeterminate; may or may not make a difference.

*Loop check (Figure 20) will stop oscillation if $R_n \ll |Z_{cf}|$ at UGBW

**Only oscillates over a portion of the output cycle.

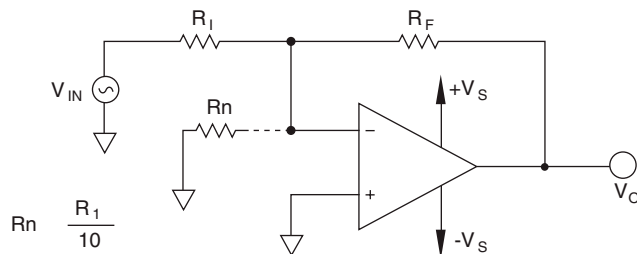


FIGURE 20. LOOP CHECK CIRCUIT

into the origin of the problem and provides guidance as to the appropriate fix.

An amplifier becomes an oscillator when two conditions are met: total phase shift reaches 360° and the amplifier has gain at this frequency. With operational amplifiers using negative feedback, half the required phase shift is provided by the inverting nature of the circuit. This means phase shift from all other sources totals a second 180° when oscillating. The crucial element here is to examine phase shift at frequencies all the way out to the intersection of open and closed loop gains. Putting it another way, just because the circuit is designed for DC only, does not preclude it from oscillating at 1MHz. Most Apex amplifiers have gain well into the MHz region and phase shifts of both amplifiers and parasitic elements grow rapidly in this area.

KEY TO PROBABLE CAUSE / POSSIBLE SOLUTION

- A. Cause: Supply feedback loop (insufficient supply bypassing).
Solution: Bypass power supplies. See Section 4.2.
- B. Cause: Supply lead inductance.
Solution: Bypass power supplies. See Section 4.2.
- C. Cause: Ground loops.
Solution: Use “Star” grounding. See Figure 21.
- D. Cause: Capacitive load reacting with output impedance (Aol pole).
Solution: Raise gain or use input R-C compensation network. See Figure 24.
- E. Cause: Inductor within the feedback loop (noise gain zero).
Solution: Use alternate feedback path. See AN#5, “Precision Magnetic Deflection,” or AN#13, “V-I Conversion.”
- F. Cause: Input capacitance reacting with high R_F (noise gain zero).
Solution: Use C_f in parallel with R_f . ($C_f = -C_{in}$). Do not use too much C_f , or you may get problem J.
- G. Cause: Output to input coupling.
Solution: Run output traces away from input traces, ground the case, bypass or eliminate R_b (the bias current compensation resistor from $-IN$ to ground)
- H. Cause: Emitter follower output reacting with capacitive load.
Solution: Use output “snubber” network. See Section 10.1.
- I. Cause: “Composite PNP” output stage with reactive load.
Solution: Use output “snubber network.” See Section 10.1.
- J. Cause: Feedback capacitance around amplifier that is not unity gain stable (integrator instability).
Solution: Reduce C_f and/or increase C_c for unity gain stability.
- K. Cause: Insufficient compensation capacitance for closed loop gain used.
Solution: Increase C_c or increase gain and/or use input R-C compensation network. See Figure 24.
- L. Cause: Servo loop stability problem.
Solution: Compensate the “front end” or “servo amplifier.”

10.1 BASICS OF STABILITY

Some basic practices must be followed to ensure stability. Proper ground practices are mandatory and are illustrated in Figure 21 (next page). Improper grounding can lead to oscillations near the unity gain bandwidth frequency of the amplifier.

Proper bypassing of power supplies is also illustrated in Figure 21. The local bypassing close to the amplifier with a small electrolytic and ceramic capacitor insure good high frequency grounding of the supply lines. The internal phase compensation on op amps will be referred to one of the supply lines and this is the reason for the importance of good local bypassing.

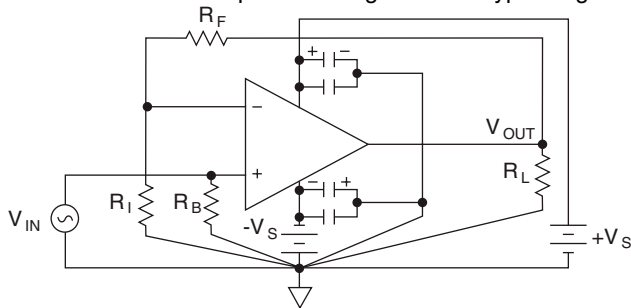


FIGURE 21. BASIC REQUIREMENTS FOR STABILITY

Table 1 shows the frequency of an oscillation is the most important clue about its source. For frequencies above unity gain the amplifier, try a snubber network as shown in Figure 22. For frequencies near the intersection of open and closed loop gains, check for weak high frequency supply bypass or for ground loops. For lower frequencies, perform a loop analysis using Application Notes 19 and 25

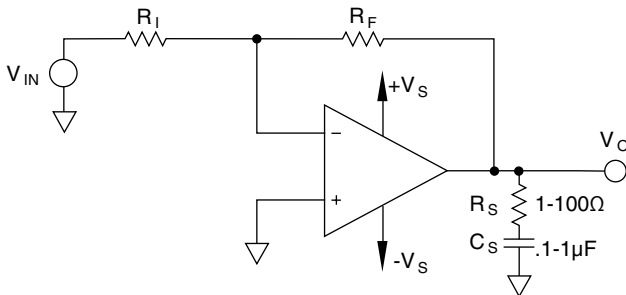


FIGURE 22. OUTPUT R-C-NETWORK ("SNUBBER")

10.2 COMMON SOURCES OF NON-LOOP INSTABILITY

The following is a list of the most common instability situations reported:

- 1) Large electrolytic or tantalum capacitors are installed close to the amplifier pins as recommended, but small ceramic bypass capacitors are omitted. The circuit may oscillate because the high frequency impedance of the large capacitors is not low enough to decouple the power supplies.
- 2) A prototype circuit is checked out and approved. A printed circuit board is built and all modes of operation test okay. A step and repeat technique then uses this same artwork to generate a multiple amplifier board. When tested, every amplifier on the board oscillates. Cross coupling through the supplies is a major problem in multiple amplifier circuits. Use lots of bypass capacitors, ground the case, and consider all items in the following section.
- 3) Ungrounded cases can cause oscillations, especially with faster amplifiers. The cases of most APEX metal can amplifiers are electrically isolated to provide mounting flexibility. The case is in close proximity to all the internal nodes of the amplifier and can act as an antenna. Providing a connection to ground prevents noise pickup, cross-coupling or positive feedback leading to oscillations. Some models have heatsink tabs connected to $-V_S$, serving the same purpose as long as $-V_S$ is clean.

- 4) A standard inverting circuit includes an impedance matching resistor in series with the non-inverting input to take advantage of the improved input offset current specification. The high impedance input becomes an antenna, receiving positive feedback, causing oscillation. Calculate the errors without using the resistor (some amplifiers have equal bias and offset currents negating the effect of the resistor). If the resistor is required, bypass it with a ceramic capacitor of at least .01uF.

10.3 LOOP STABILITY ISSUES

A majority of loop instability problems are due to one or more of the following:

- 1) Amplifier compensation not matched to the circuit closed loop gain. This includes using amplifiers below their recommended gain, choosing the wrong external compensation or failure to realize high frequency (not DC) gain is what counts. (A feedback or integrating capacitor lowers gain at high frequency).
- 2) The use of large impedance values for input or feedback networks allows parasitic elements too much control. Consider a 100KΩ feedback resistor with a parasitic of 3pF. This places a pole (with an additional 45° phase shift) at about 53KHz!
- 3) Capacitive loads reacting with amplifier output impedance, effectively adding a pole and corresponding phase shift to the amplifier.
- 4) Voltage-to-current phase shift of an inductor is inside the feedback loop of current output circuits.
- 5) Too many amplifiers inside a single loop. Each amplifier contributes to the total as you go around the loop.

Solutions for these include one or more of the following:

- 1) Change to an amplifier suitable for lower gain, increase external phase compensation, or modify the circuit.
- 2) Lower impedance values.
- 3) Add an isolation resistor outside the feedback loop to defeat the effect of the capacitive load as shown in Figure 23. This is the simplest external component solution and has surprisingly little effect on circuit performance.

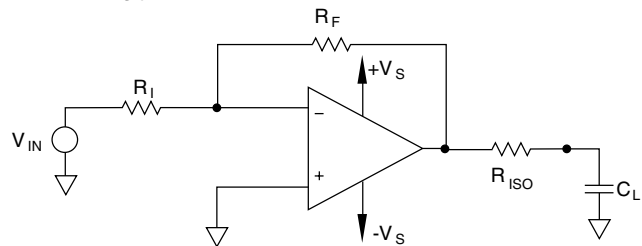


FIGURE 23. CAPACITIVE LOAD ISOLATION

- 4) Increase DC closed loop gain.
- 5) Increase AC gain only with noise gain compensation as shown in Figure 24 (next page). This technique works well with inverting circuits but is not recommended for non-inverting circuits.
- 6) Lower the intersection rate of open and closed loop gains with a properly sized roll off capacitor. Usually, bigger is not better.
- 7) Add an AC voltage gain limiter to the current output circuit. At the higher frequencies where the inductor demands very high voltages, this R-C network puts the amplifier into a voltage feedback mode.
- 8) Lower amplifier count.

Most of these solutions tend to negatively impact bandwidth, especially in the current output circuits. Apex has been known

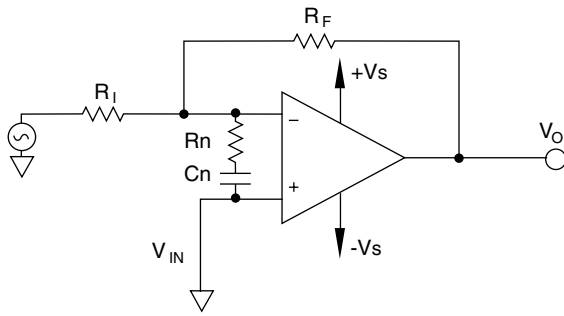


FIGURE 24. INPUT R-C NETWORK COMPENSATION

to boast, "Any circuit can be made stable". Notice that bandwidth trade offs were not part of the quotation; this is where the engineering work lies. Upon looking at the Application Notes mentioned above, some of you may be thinking about the amount of this work, with phrases we can't print here. Have no fear, Power Design takes care of all the tedious math and graphing for you making design iterations a snap.

10.4 A FINAL STABILITY NOTE

When you're at your wits end trying to solve an oscillation problem, don't give up because you have it down to an "acceptably low" level. A circuit either oscillates or it doesn't, and no amount of oscillation is acceptable. Apply these techniques and ideas under your worst case load conditions and you can conquer your oscillation problems.

THE APEX APPLICATIONS HOTLINE

The APEX Applications Hotline provides technical support all the way through your project. In many cases, specific failure prevention can be suggested immediately. In some instances we will need the amplifier to be sent to APEX for a failure analysis. The results of the analysis can pinpoint the area of damage which then narrows down the circuit problem.